### UNITRODE



UC1841 UC2841 UC3841

## Programmable, Off-Line, PWM Controller

### **FEATURES**

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-current, Off-line Start Circuit
- Voltage Feed Forward or Current Mode Control
- Guaranteed Duty Cycle Clamp
- PWM Latch for Single Pulse per Period
- Pulse-by-Pulse Current Limiting Plus Shutdown for Over-Current Fault
- No Start-up or Shutdown Transients
- Slow Turn-on Both Initially and After Fault Shutdown
- Shutdown Upon Over- or Under-Voltage Sensing
- Latch Off or Continuous Retry After Fault
- PWM Output Switch Usable to 1A Peak Current
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL Package

### **DESCRIPTION**

The UC1841 family of PWM controllers has been designed to increase the level of versatility while retaining all of the performance features of the earlier UC1840 devices. While still optimized for highly-efficient bootstrapped primary-side operation in forward or flyback power converters, the UC1841 is equally adept in implementing both low and high voltage input DC to DC converters. Important performance features include a low-current starting circuit, linear feed-forward for constant volt-second operation, and compatibility with either voltage or current mode topologies.

In addition to start-up and normal regulating PWM functions, these devices include built in protection from over-voltage, under-voltage, and over-current fault conditions with the option for either latch-off or automatic restart.

While pin compatible with the UC1840 in all respects except that the polarity of the External Stop has been reversed, the UC1841 offers the following improvements:

- 1. Fault latch reset is accomplished with slow start discharge rather than recycling the input voltage to the chip.
- 2. The External Stop input can be used for a fault delay to resist shutdown from short duration transients.
- 3. The duty-cycle clamping function has been characterized and specified.

The UC1841 is characterized for -55°C to +125°C operation while the UC2841 and UC3841 are designed for -25°C to +85°C and 0°to +70°C, respectively.

#### **BLOCK DIAGRAM** VIN SENSE -11 RAMP 10 RAMP GEN CLOCK osc VIN SUPPLY RT/CT 9 DRIVE SWITCH DRIVER BIAS CIRCUIT COMP 1 INV. INPUT 17 REF GEN AND BIAS SUPPLY PWM AMP -16 5.0V REF 400本 NI INPUT 18 START/UV 2 R сомр 200 μA **HYSTERESIS** OR<sub>2</sub> - 5 RESET **CURRENT LIMIT** INT. 3.0V REF 6 THRESHOLD 0.4V CURRENT 7 SENSE SLOW-START/ DUTY CYCLE CLAMP R 400mV ☆ 6٧ SERROR OV SENSE 3 ■ GROUND 3V REF OR3 OR1 EXT. STOP 4 Note: Positive true logic, latch outputs high with set, reset has priority.

### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, +V <sub>IN</sub> (Pin 15) (Note 2)
Voltage Driven
Current Driven, 100mA maximum Self-limiting
PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20μJoules
Driver Bias Current (Pin 14)200mA
Reference Output Current (Pin 16)50mA
Slow-Start Sink Current (Pin 8) 20mA
VIN Sense Current (Pin 11)
Current Limit Inputs (Pins 6 & 7)0.5 to +5.5V
Stop Input (Pin 4)0.3 to +5.5V
Comparator Inputs
(Pins 1, 7, 9-11, 16) Internally clamped at 12V
Power Dissipation at T <sub>A</sub> = 25°C (Note 3) 1000mW

Power Dissipation at Tc = 25°C (Note 3)........... 2000mW

### **CONNECTION DIAGRAMS**

DIL-18, SOIC-18 (TOP VIEW) J or N, DW Package						
Comp 1	18 N.I. Input					
Start/UV 2	17 Inv. Input					
OV Sense 3	16 5.0V Ref.					
Stop 4	15 +Vin Supply					
Reset 5	14 Drive Bias					
Cur Thresh 6	13 Ground					
Cur Sense 7	12 PWM Out					
Slow Start 8	11 Vin Sense					
RT/CT 9	10 Ramp					

Operating Junction Temperature55°C to +150°C					
Storage Temperature Range65°C to +150°C					
Lead Temperature (Soldering, 10 sec) +300°C					
Note 1: All voltages are with respect to ground, Pin 13.					
Currents are positive-into, negative-out of the specified					

Currents are positive-into, negative-out of the specified terminal.

Note 2: All pin numbers are referenced to DIL-18 package. Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

PLCC-20, LCC-20	PACKAGE PIN FUNCTIONS					
(TOP VIEW) Q or L Package	FUNCTION	PIN				
Q of L Package	Comp	1				
	Start/UV	2				
	OV Sense	3				
	Stop	4				
3 2 1 20 19	Reset	5				
4 18	CUR Thresh	7				
5 17	CUR Sense	8				
6 16	Slow Start	9				
7 15	RT/CT	10				
8 14	Ramp	11				
9 10 11 12 13	Vin Sense	12				
	PWM Out	13				
	Ground	14				
	Drive Bias	15				
	+Vin Supply	17				
	5.0V REF	18				
	Inv. Input	19				
	N.I. Input	20				

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for Ta = -55°C to +125°C for the UC1841, -25°C to +85°C for the UC2841, and 0°C to +70°C for the UC3841; Vin = 20V, RT =  $20k\Omega$ , CT = .001mfd, RR =  $10k\Omega$ , CR = .001mfd, Current Limit Threshold = 200mV, Ta = TJ.

PARAMETER TEST CONDITIONS		UC1	841 / UC	2841		UC3841	C3841	
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	
Power Inputs								
Start-Up Current	VIN = 30V, Pin 2 = 2.5V		4.5	6		4.5	6	mA
Operating Current	VIN = 30V, Pin 2 = 3.5V		10	14		10	14	mA
Supply OV Clamp	IIN = 20mA	33	40	45	33	40	45	V
Reference Section								
Reference Voltage	T <sub>J</sub> = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	VIN = 8 to 30V		10	15		10	20	mV
Load Regulation	IL = 0 to 10mA		10	20		10	30	mV
Temperature Stability	Over Operating Temperature Range	4.9		5.1	4.85		5.15	V
Short Circuit Current	VREF = 0, T <sub>J</sub> = 25°C		-80	-100		-80	-100	mA
Oscillator	•	-	•	*	-	•	•	-
Nominal Frequency	T <sub>J</sub> = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	VIN = 8 to 30V		0.5	1		0.5	1	%
Temperature Stability	Over Operating Temperature Range	45		55	43		57	kHz
Maximum Frequency	$RT = 2k\Omega$ , $CT = 330pF$	500			500			kHz

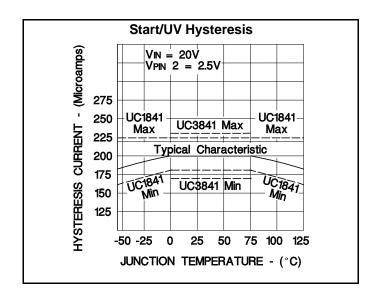
**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for the UC1841, -25°C to +85°C for the UC2841, and 0°C to +70°C for the UC3841; ViN = 20V, RT =  $20k\Omega$ , CT = .001mfd, RR =  $10k\Omega$ , CR = .001mfd, Current Limit Threshold = 200mV, TA = TJ.

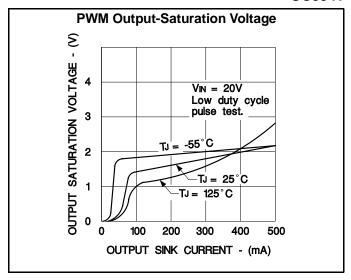
Ramp Generator  Ramp Current, Minimum  Ramp Current, Maximum  Ramp Valley  Ramp Peak  Clamping Level  Error Amplifier  Input Offset Voltage  Input Bias Current  Open Loop Gain  Output Swing (Max. Output ≤ Ramp Peak - 100mV)  CMRR  PSRR  Vom = 1.5 to 5.5V  PSRR  Vin = 8 to 30V  Short Circuit Current  Vcomp = 0V  Gain Bandwidth*  Tj = 25°C, Avol = 0dB  Slew Rate*  Tj = 25°C, Avol = 0dB  PWM Section  Continuous Duty Cycle Ramp Peak < 4.2V	-0.9 0.3	-11	MAX	MIN	TYP	MAX	
Ramp Current, Minimum  Ramp Current, Maximum  Ramp Valley  Ramp Peak  Clamping Level  Error Amplifier  Input Offset Voltage Input Bias Current  Open Loop Gain  Output Swing (Max. Output ≤ Ramp Peak - 100mV)  CMRR  PSRR  VCM = 1.5 to 5.5V  PSRR  VIN = 8 to 30V  Short Circuit Current  Vcomp = 0V  Gain Bandwidth*  TJ = 25°C, AvoL = 0dB  PWM Section  Continuous Duty Cycle Range* (other than zero)  Minimum Total Continuous Range, Ramp Peak < 4.2V		-11		-			
Ramp Current, Maximum       ISENSE = 1.0mA         Ramp Valley       Clamping Level         Error Amplifier       VCM = 5.0V         Input Offset Voltage       VCM = 5.0V         Input Bias Current       Duput Bias Current         Input Offset Current       Doen Loop Gain         Output Swing (Max. Output ≤ Ramp Peak - 100mV)       Minimum Total Range         CMRR       VCM = 1.5 to 5.5V         PSRR       VIN = 8 to 30V         Short Circuit Current       VCOMP = 0V         Gain Bandwidth*       TJ = 25°C, AVOL = 0dB         Slew Rate*       TJ = 25°C, AVCL = 0dB         PWM Section       Minimum Total Continuous Range, Ramp Peak < 4.2V		-11					
Ramp Valley       Clamping Level         Error Amplifier       VcM = 5.0V         Input Offset Voltage       VcM = 5.0V         Input Bias Current       Input Offset Current         Open Loop Gain       ΔVo= 1 to 3V         Output Swing (Max. Output ≤ Ramp Peak - 100mV)       Minimum Total Range         CMRR       VcM = 1.5 to 5.5V         PSRR       VIN = 8 to 30V         Short Circuit Current       VcOMP = 0V         Gain Bandwidth*       TJ = 25°C, AvoL = 0dB         Slew Rate*       TJ = 25°C, AvcL = 0dB         PWM Section       Minimum Total Continuous Range, Ramp Peak < 4.2V			-14		-11	-14	μΑ
Ramp Peak       Clamping Level         Error Amplifier       VcM = 5.0V         Input Offset Voltage       VcM = 5.0V         Input Bias Current       Description         Open Loop Gain       ΔVo= 1 to 3V         Output Swing (Max. Output ≤ Ramp Peak - 100mV)       Minimum Total Range         CMRR       VcM = 1.5 to 5.5V         PSRR       VIN = 8 to 30V         Short Circuit Current       VcOMP = 0V         Gain Bandwidth*       TJ = 25°C, AvoL = 0dB         Slew Rate*       TJ = 25°C, AvcL = 0dB         PWM Section       Minimum Total Continuous Range, Ramp Peak < 4.2V	0.3	95		-0.9	95		mA
Error Amplifier         Input Offset Voltage       VcM = 5.0V         Input Bias Current       VcM = 5.0V         Input Offset Current       AVo= 1 to 3V         Output Swing (Max. Output ≤ Ramp Peak - 100mV)       Minimum Total Range         CMRR       VcM = 1.5 to 5.5V         PSRR       VIN = 8 to 30V         Short Circuit Current       VcOMP = 0V         Gain Bandwidth*       TJ = 25°C, AvoL = 0dB         Slew Rate*       TJ = 25°C, AvcL = 0dB         PWM Section         Continuous Duty Cycle Range* (other than zero)       Minimum Total Continuous Range, Ramp Peak < 4.2V	5.0	0.4	0.6	0.3	0.4	0.6	V
Input Offset Voltage       Vcм = 5.0V         Input Bias Current       Input Offset Current         Open Loop Gain       ΔVo= 1 to 3V         Output Swing (Max. Output ≤ Ramp Peak - 100mV)       Minimum Total Range         CMRR       Vcм = 1.5 to 5.5V         PSRR       VIN = 8 to 30V         Short Circuit Current       VcomP = 0V         Gain Bandwidth*       TJ = 25°C, AvoL = 0dB         Slew Rate*       TJ = 25°C, AvcL = 0dB         PWM Section         Continuous Duty Cycle Range* (other than zero)       Minimum Total Continuous Range, Ramp Peak < 4.2V	3.9	4.2	4.5	3.9	4.2	4.5	V
Input Bias Current         Input Offset Current         Open Loop Gain       ΔVo= 1 to 3V         Output Swing (Max. Output ≤ Ramp Peak - 100mV)       Minimum Total Range         CMRR       Vcм = 1.5 to 5.5V         PSRR       VIN = 8 to 30V         Short Circuit Current       Vcomp = 0V         Gain Bandwidth*       TJ = 25°C, AvoL = 0dB         Slew Rate*       TJ = 25°C, AvcL = 0dB         PWM Section         Continuous Duty Cycle Range* (other than zero)       Minimum Total Continuous Range, Ramp Peak < 4.2V	•				,		
$\begin{array}{llllllllllllllllllllllllllllllllllll$		0.5	5		2	10	mV
$ \begin{array}{llllllllllllllllllllllllllllllllllll$		0.5	2		1	5	μΑ
$\begin{array}{lll} & \text{Output Swing (Max. Output} \leq \\ & \text{Ramp Peak - 100mV)} & \text{Minimum Total Range} \\ & \text{CMRR} & \text{VcM} = 1.5 \text{ to } 5.5 \text{V} \\ & \text{PSRR} & \text{VIN} = 8 \text{ to } 30 \text{V} \\ & \text{Short Circuit Current} & \text{VcOMP} = 0 \text{V} \\ & \text{Gain Bandwidth*} & \text{TJ} = 25 ^{\circ}\text{C}, \text{ AVoL} = 0 \text{dB} \\ & \text{Slew Rate*} & \text{TJ} = 25 ^{\circ}\text{C}, \text{ AVcL} = 0 \text{dB} \\ & \text{\textbf{PWM Section}} \\ & \text{Continuous Duty Cycle} & \text{Minimum Total Continuous Range,} \\ & \text{Range* (other than zero)} & \text{Ramp Peak} < 4.2 \text{V} \\ & \text{Automode of the continuous Range,} \\ & \text{Ramp Peak} < 4.2 \text{V} \\ \\ \\ & \text{Ramp Peak} < 4.2 \text{V} \\ \\ \\ &$			0.5			0.5	μΑ
Ramp Peak - 100mV)         VcM = 1.5 to 5.5V           CMRR         VcM = 1.5 to 5.5V           PSRR         VIN = 8 to 30V           Short Circuit Current         Vcomp = 0V           Gain Bandwidth*         TJ = 25°C, Avol = 0dB           Slew Rate*         TJ = 25°C, Avcl = 0dB           PWM Section         Minimum Total Continuous Range, Ramp Peak < 4.2V	60	66		60	66		dB
$\begin{array}{lll} \text{PSRR} & \text{VIN} = 8 \text{ to } 30 \text{V} \\ \text{Short Circuit Current} & \text{VCOMP} = 0 \text{V} \\ \text{Gain Bandwidth*} & \text{TJ} = 25 ^{\circ}\text{C},  \text{AVoL} = 0 \text{dB} \\ \text{Slew Rate*} & \text{TJ} = 25 ^{\circ}\text{C},  \text{AVcL} = 0 \text{dB} \\ \hline \textbf{PWM Section} & \\ \text{Continuous Duty Cycle} & \text{Minimum Total Continuous Range,} \\ \text{Range*} & \text{(other than zero)} & \text{Ramp Peak} < 4.2 \text{V} \\ \end{array}$	0.3		3.5	0.3		3.5	V
$ \begin{array}{llllllllllllllllllllllllllllllllllll$	70	80		70	80		dB
$\begin{tabular}{lll} Gain Bandwidth* & T_J = 25 °C, Avol = 0 dB \\ Slew Rate* & T_J = 25 °C, Avol = 0 dB \\ \hline {\bf PWM Section} & \\ Continuous Duty Cycle & Minimum Total Continuous Range, Ramp Peak < 4.2V } \\ \hline \end{tabular}$	70	80		70	80		dB
Slew Rate* TJ = 25°C, AvcL = 0dB  PWM Section  Continuous Duty Cycle Range* (other than zero)  Minimum Total Continuous Range, Ramp Peak < 4.2V		-4	-10		-4	-10	mA
PWM Section  Continuous Duty Cycle Range* (other than zero)  Minimum Total Continuous Range, Ramp Peak < 4.2V	1	2		1	2		MHz
Continuous Duty Cycle Minimum Total Continuous Range, Ramp Peak < 4.2V		0.8			0.8		V/μs
Range* (other than zero) Ramp Peak < 4.2V	•						
	4		95	4		95	%
50% Duty Cycle Clamp Rsense to Vref = 10k	42	47	52	42	47	52	%
Output Saturation IouT = 20mA		0.2	0.4		0.2	0.4	V
IOUT = 200mA		1.7	2.2		1.7	2.2	V
Output Leakage Vout = 40V		0.1	10		0.1	10	μΑ
Comparator Delay* Pin 8 to Pin 12, TJ = 25°C, RL = 1kΩ	Ω	300	500		300	500	ns
Sequencing Functions							
Comparator Thresholds Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current Pins 3, 5 = 0V		-1.0	-4.0		-1.0	-4.0	μΑ
Input Leakage Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	μΑ
Start/UV Hysteresis Current Pin 2 = 2.5V	170	200	220	170	200	230	μΑ
Ext. Stop Threshold Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	V
Error Latch Activate Current Pin 4 = 0V, Pin 3 > 3V		-120	-200		-120	-200	μΑ
Driver Bias Saturation Voltage, VIN - VOH		2	3		2	3	V
Driver Bias Leakage VB = 0V		-0.1	-10		-0.1	-10	μΑ
Slow-Start Saturation Is = 10mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage Vs = 4.5V		0.1	2.0		0.1	2.0	μΑ
Current Control							
Current Limit Offset		0	5		0	10	mV
Current Shutdown Offset	370	400	430	360	400	440	mV
Input Bias Current Pin 7 = 0V		2	_		2	-5	μΑ
Common Mode Range*		-2	-5		-2	-5	μιτ
Current Limit Delay* $T_J = 25^{\circ}C$ , Pin 7 to 12, RL = 1k	-0.4	-2	-5 3.0	-0.4	-2	3.0	V

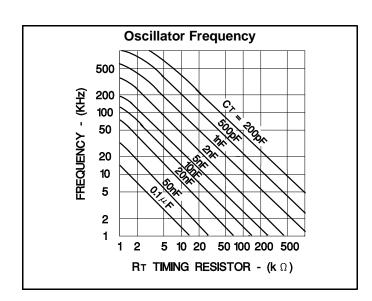
<sup>\*</sup> These parameters are guaranteed by design but not 100% tested in production.

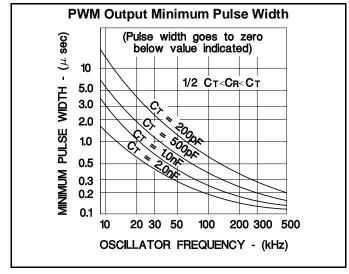
### **FUNCTIONAL DESCRIPTION**

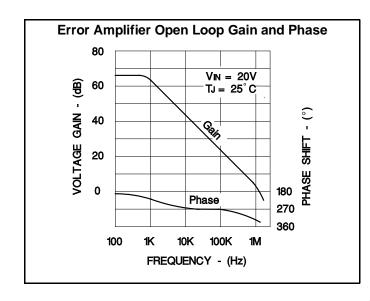
PWM CONTROL	
1. Oscillator	Generates a fixed-frequency internal clock from an external RT and CT.
	Frequency = $\frac{K_C}{R_TC_T}$ where Kc is a first order correction factor $\approx 0.3 \log (C_T \times 10^{12})$ .
2. Ramp Generator	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{\text{RRCR}}$
	CR is normally selected ≤ CT and its value will have some effect upon valley voltage.  Limiting the minimum value for ISENSE will establish a maximum duty cycle clamp.  CR terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation.  Low output impedance; unity-gain stable.  The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of $\pm$ 2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
SEQUENCING FUNCTIONS	<u> </u>
1. Start/UV Sense	With an increasing voltage, it generates a turn-on signal and releases the slow-start clamp at a start threshold.  With a decreasing voltage, it generates a turn-off command at a lower level separated by a
2. Drive Switch	200µA hysteresis current.  Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by RsCs for slow increase of output pulse width.  Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	our also be used as air alternate maximum daty byte clamp with air external voltage divider.
1. Error Latch	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (typically 3V) b. Stop > 2.4V (typically 1.6V) c. Current Sense 400mV over threshold (typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin 5 < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set.
2. Current Limiting	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold.  When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch.
3. External Stop	A voltage over 1.2V will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a typical delay of 13ms/μF.

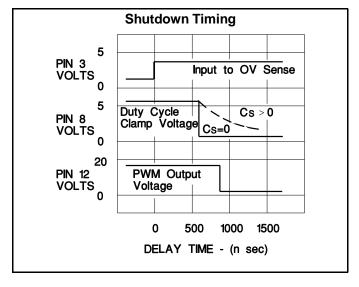




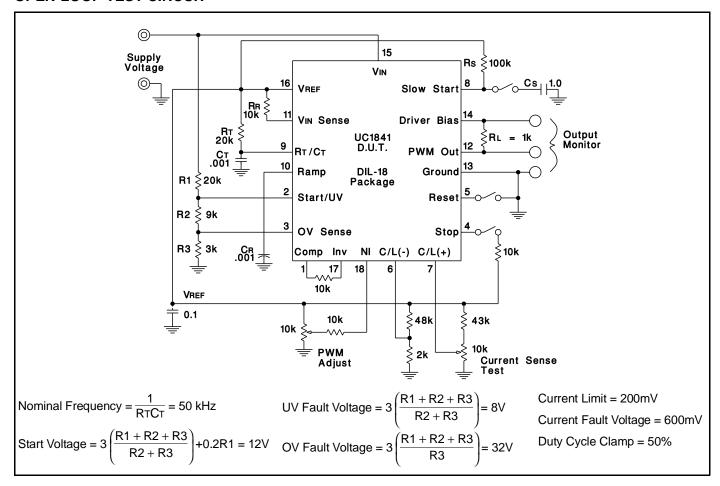








### **OPEN-LOOP TEST CIRCUIT**



### **FLYBACK APPLICATION (A)**

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by RIN and CIN during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling — a task made even easier with the UC1841's feed-forward line regulation.

An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output.

Not shown, are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application; however, one example of power transistor interfacing is provided on the following page.

### **REGULATOR APPLICATION (B)**

With the addition of a level shifting transistor, Q1, the UC1841 is an ideal control circuit for DC to DC converters such as the buck regulator shown in Figure B opposite. In addition to providing constant current drive pulses to the PIC661 power switch, this circuit has full fault protection and high speed dynamic line regulation due to its feedforward capability. An additional feature is the ability to

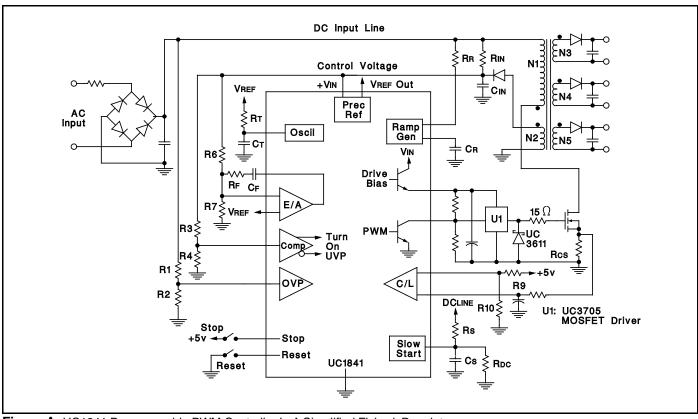


Figure A. UC1841 Programmable PWM Controller In A Simplified Flyback Regulator

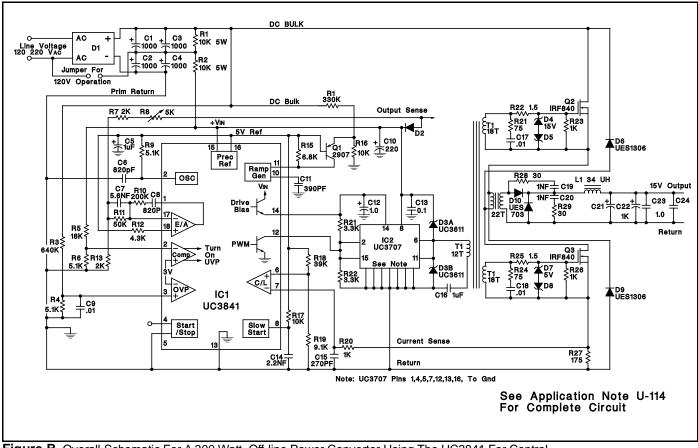
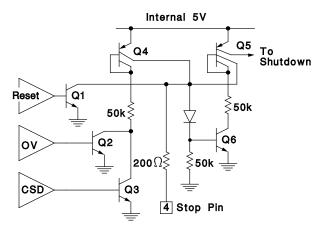


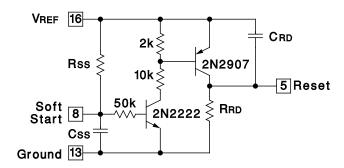
Figure B. Overall Schematic For A 300 Watt, Off-line Power Converter Using The UC3841 For Control

### **ERROR LATCH INTERNAL CIRCUITRY**



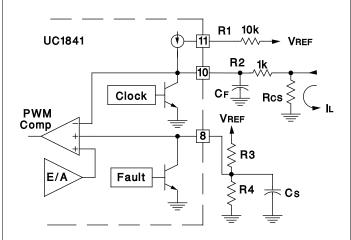
The Error Latch consists of Q5 and Q6 which, when both on, turns off the PWM Output and pulls the Slow-Start pin low. This latch is set by either the Over-Voltage or Current Shutdown comparators, or by a high signal on Pin 4. Reset is accomplished by either the Reset comparator or a low signal on Pin 4. An activation time delay can be provided with an external capacitor on Pin 4 in conjunction with the  $\approx 100 \mu A$  collector current from Q4.

# PROGRAMMABLE SOFT START AND RESTART DELAY CIRCUIT



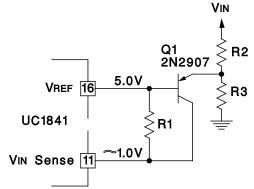
Restart Delay = (.51)(RRD)(CRD)

### **CURRENT MODE CONTROL**



Since Pin 10 is a direct input to the PWM comparator, this point can also serve as a current sense port for current mode control. In this application, current sensing is ground referenced through Rcs. Resistor R1 sets a 400mV offset across R2 (assuming R2 > Rcs) so that both the Error Amplifier and Fault Shutdown can force the current completely to zero. R2 is also used along with CF as a small filter to attenuate leading-edge spikes on the load current waveform. In this mode, current limiting can be accomplished by divider R3/R4 which forms a clamp overriding the output of the Error Amplifier.

# VOLTAGE FEED-FORWARD COMBINED WITH MAXIMUM DUTY-CYCLE CLAMP



In this circuit, R1 is used in conjunction with CR (not shown) to establish a minimum ramp charging current such that the ramp voltage reaches 4.2V at the required maximum output pulse width.

The purpose of Q1 is to provide an increasing ramp current above a threshold established by R2 and R3 such that the duty cycle is further reduced with increasing Vin.

The minimum ramp current is:

$$IR(MIN) = \frac{VREF - VIN SENSE}{R_1} \approx \frac{4V}{R_1}$$

The threshold where VIN begins to add extra ramp current is:

$$VIN \approx 5.6V \left( \frac{R2 + R3}{R3} \right)$$

Above the threshold, the ramp current will be:

IR (VARIAB) 
$$\approx \frac{4}{R1} + \frac{VIN - 5.6}{R2} - \frac{5.6}{R3}$$

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to Customer on an annual basis.







### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp (3)
5962-8992002VA	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC1841J	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC1841J883B	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC1841L	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
UC1841L883B	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
UC2841DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2841DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2841J	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC2841N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2841NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3841DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3841DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3841DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3841DWTRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3841J	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC3841N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3841NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

 $^{(1)}$  The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## **PACKAGE OPTION ADDENDUM**

18-Sep-2008

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3841DWTR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1





### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3841DWTR	SOIC	DW	18	2000	346.0	346.0	41.0

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